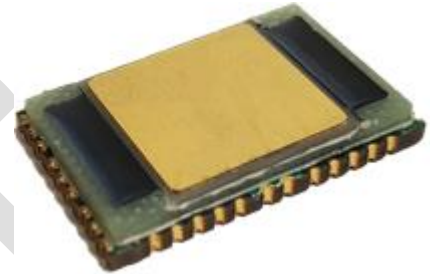

TECHNICAL DATA

Datasheet 6150, PRELIMINARY

GaN FET Half-Bridge with Gate Driver

FEATURES:

- 350VDC Rating
- Isolated top-side cooling
- Package Size 1.10" x 0.70" x 0.14"
- High side floating bootstrap configuration
- Anti-cross conduction protection
- Low voltage logic level input compatible
- Junction Temperature Range -55°C TO +150°C
- Designed for commercial, industrial, and aerospace applications.



DESCRIPTION:

This GaN FET Half Bridge module is a completely self-contained power module that can be used in various power applications including, but not limited to, motor drivers and DC-DC converters requiring high-frequency designs. Built in cross conduction dead time between high and low side signals protects the output stage from shoot-through. The module includes a bootstrapped floating gate driver for the high side FET. Each GaN FET is conduction cooled through proprietary isolated, top-side cooling technology.

The small size of this complete module makes it ideal for high reliability commercial, aerospace, and military applications.

TECHNICAL DATA

Datasheet 6150, PRELIMINARY

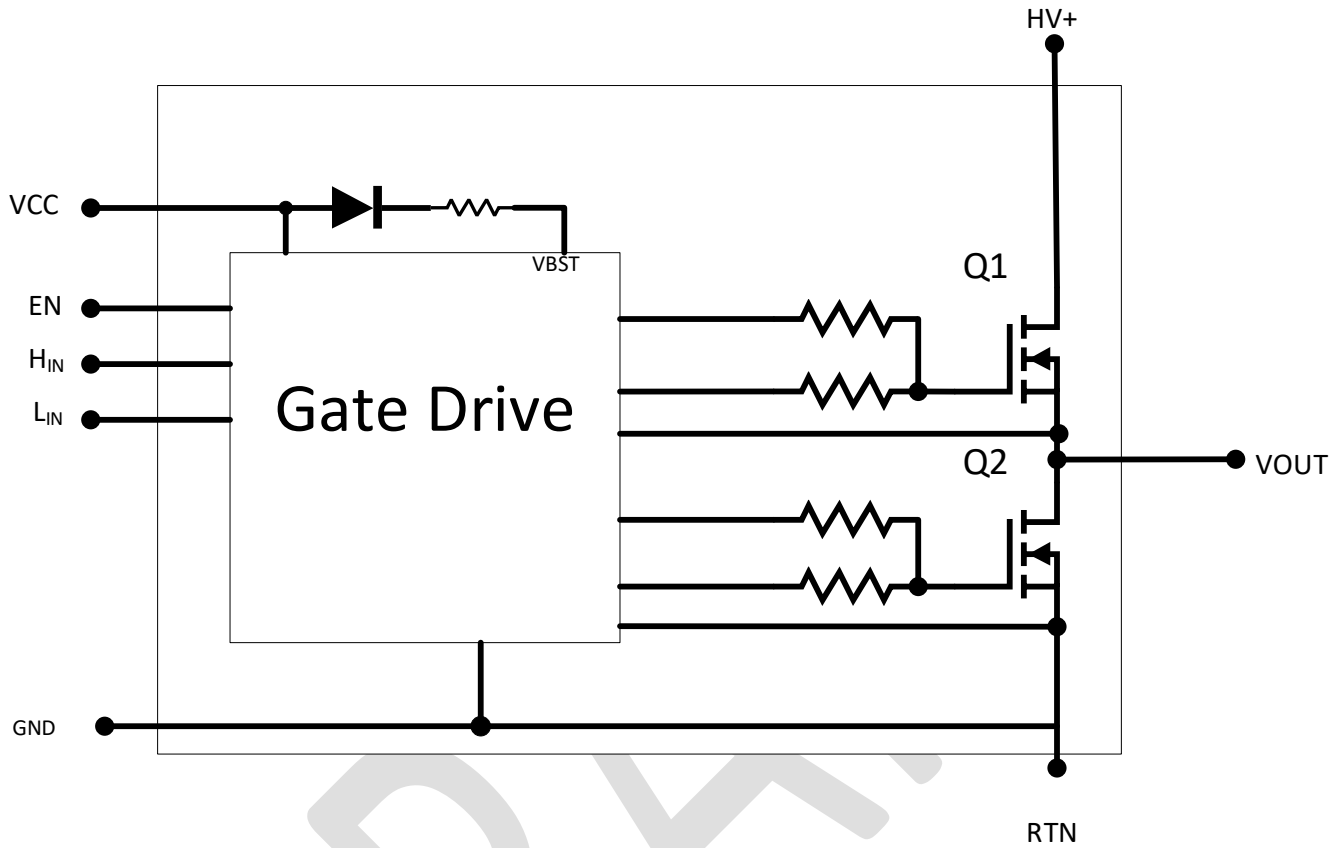


Figure 1 – Block Diagram

TECHNICAL DATA

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ABSOLUTE MAXIMUM RATINGS

(T_c = 25 °C unless otherwise noted, Q1 and Q2)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Drain-to-Source Breakdown Voltage	BV _{DSS}		350	V
Pulsed Drain Current, Pulse Width limited to 300 μsec	I _{DM}		120	A
Power Dissipation, T _c = 25°C	P _{25C}		50	W
Power Dissipation, T _c = 80°C	P _{80C}		28	W
Supply Voltage	V _{CC}	-0.3	20	V
Logic Input Voltage	HIN, LIN, EN	-0.3	20	V
Maximum Operating Junction Temperature	T _{Jmax}	-55	150	°C
Maximum Storage Junction Temperature	T _{Jmax}	-55	150	°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance, Junction to Case, half-bridge	R _{θJC}			2.5	°C/W

TECHNICAL DATA

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ELECTRICAL CHARACTERISTICS

(T_C = 25 °C, V_{CC} = +15V unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
INPUT STAGE (Referenced to GND)				
Input Supply Current I _{CC} at V _{CC} =+15V supply without PWM Signals, EN = 0V		100	150	μA
Low input PWM at 500kHz		1.5	2.5	mA
V _{CC} Input Supply Voltage Range (Recommended)	9		17	V
V _{CC} Under Voltage Lockout Positive Going Threshold	8.0	8.5	9.0	V
V _{CC} Under Voltage Lockout Negative Going Threshold	7.5	8.0	8.5	V
V _{CC} Under Voltage Lockout Hysteresis		0.5		V
Logic Input Voltage High V _{INH} HIN, LIN and EN			2.5	V
Logic Input Voltage Low V _{INL} HIN, LIN and EN	1.2			V
Input Logic Voltage Hysteresis		0.5		V
High Level Logic Input Bias Current I _{IN+} HIN, LIN and EN V _{HIN} = V _{LIN} = 5V	9	15	21	μA
Low Level Logic Input Bias Current I _{IN-} HIN, LIN and EN V _{HIN} = V _{LIN} = 0V			2.2	μA
Input Pull-Down Resistance R _{IN} HIN, LIN and EN V _{HIN} = V _{LIN} = 5V		333		kΩ
POWER OUTPUT STAGE, Q1 AND Q2				
Drain-to-Source Voltage, V _{GS} = 0V, I _D = 320μA, BV _{DSS}	350			V
Static Drain-to-Source On-Resistance, R _{DS(on)}		15	30	mΩ
Reverse Leakage Current, V _{DS} = 280V, V _{GS} = 0V, I _{DSS}		8	300	μA
Source-to-Drain Forward Voltage, I _S = 2A, V _{GS} = 0V, V _{SD}		1.5		V

TECHNICAL DATA

Datasheet 6150, PRELIMINARY

ELECTRICAL CHARACTERISTICS (continued)

($T_C = 25\text{ }^\circ\text{C}$, $V_{CC} = +15\text{V}$ unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS				
At 220V, $I_{out} = 25\text{A}$, pulsed				
Turn-on Propagation Delay, Upper or Lower FET, t_{don} Measured from Logic input crossing 50% to I_D rising to 90%		25	55	nsec
Turn-off Propagation Delay, Upper or Lower FET, t_{doff} Measured from Logic input crossing 50% to I_D falling to 10%		25	55	nsec
Turn-on Transition Time, Upper or Lower FET, t_{ri} I_D rising from 10% to 90%		5	10	nsec
Turn-off Transition Time, Upper or Lower FET, t_{fi} I_D falling from 90% to 10%		5	10	nsec
Dead Time ¹				

¹Anti-cross-conduction is provided; dead time is only inserted if input signals overlap, equal to the amount of overlap time. Additional dead time should be provided by the user.

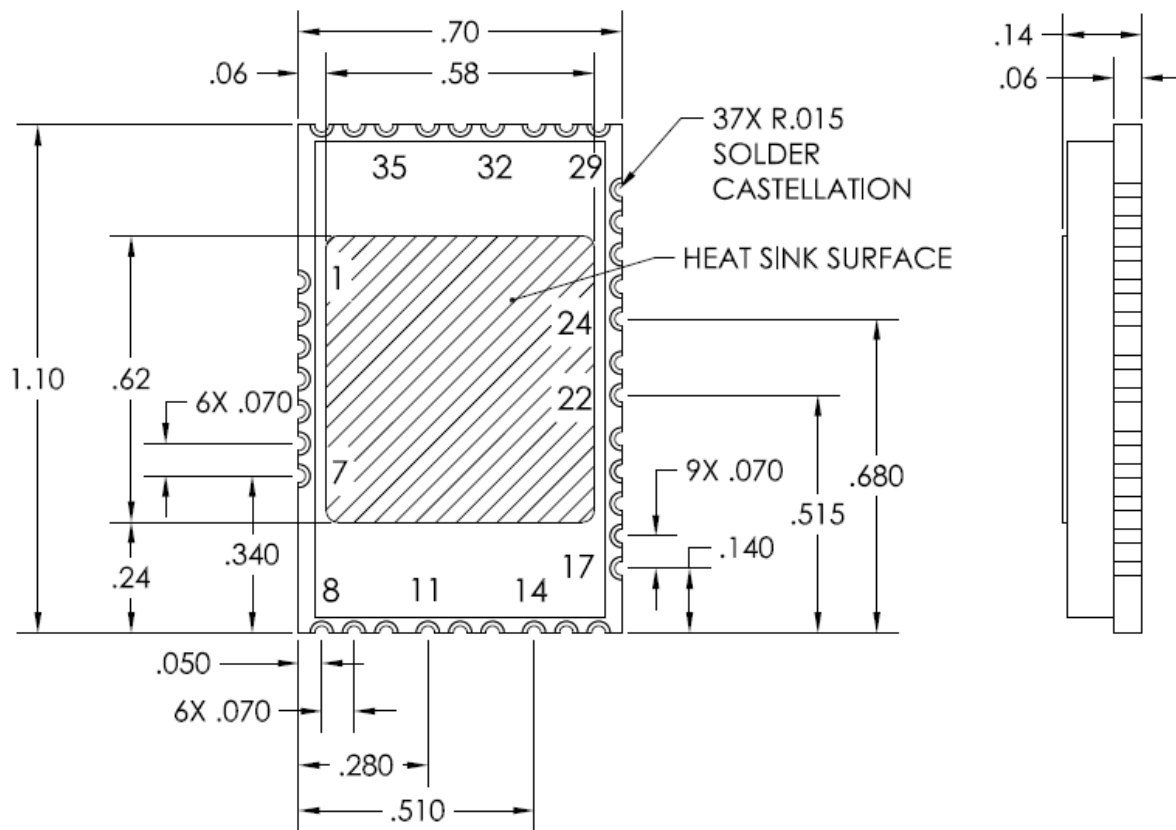
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Figure 2 - Package Drawing Top & Side Views

Notes:

1. Selective solder with solder iron, laser soldering, or similar process with Sn63/ Pb37 solder alloy. Maximum temperature of 260°C for 10 seconds maximum per castellation. Pre-heat board to 80-100°C to aid soldering when being attached to copper planes. Do not pass through a SMT reflow furnace.
2. Board must be conformal coated after installation.

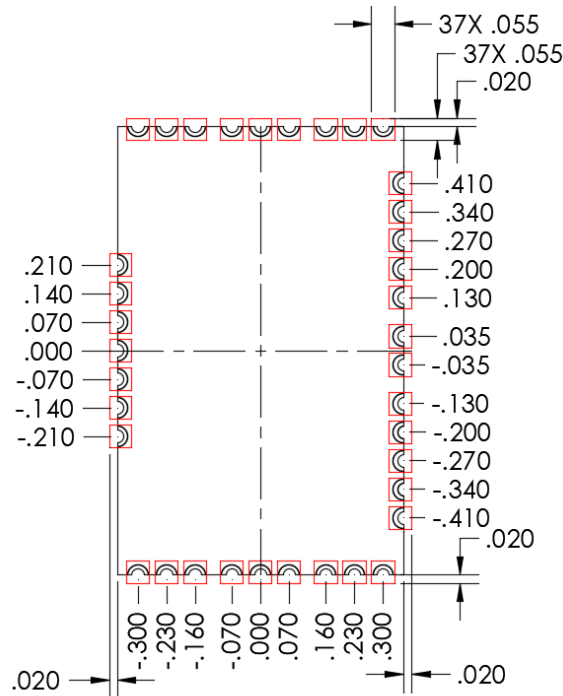


DIMENSIONS IN INCHES
TOLERANCE UNLESS OTHERWISE NOTED
.XX = ±.01
.XXX = ±.005

TECHNICAL DATA

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**Figure 3 – Suggested PCB Footprint
Top view**



PIN OUT

Castellation #	Name	Description
1-2, 4	GND	Logic Ground Return Point
3	V _{CC}	Logic Input Power Supply
5	L _{IN}	Low Side FET Logic Input Control
6	H _{IN}	High Side FET Logic Input Control
7	EN	Enable Signal Logic Input Control
11-13, 32-34	RTN	High Voltage Bus Return
8-10, 14-16, 22-23, 29-31, 35-37	V _{OUT}	Half Bridge High Voltage Output
17-21, 24-28	HV+	High Voltage DC Bus

TECHNICAL DATA

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